REMARKS

Summary of Claim Status

Claims 1-4, 6-17, 22, and 24-28 are pending in the present application after entry of the present amendment. Claims 1-4, 6, 8, 9, 12-17, 22, and 24-28 are rejected for the reasons discussed below. Claims 7, 10, and 11 are objected to as depending from a rejected base claim, but indicated as allowable if properly rewritten in independent form. Applicants thank the Examiner for this acknowledgement of patentable subject matter.

Applicants respectfully request favorable reconsideration of the claims and withdrawal of the pending rejections and objections in view of the present amendment and in light of the following discussion.

Rejections Under 35 U.S.C. § 102

Claims 1, 2, 4, 12-17, 22, 24, 26, and 28 are rejected under 35 U.S.C. § 102(b) as being anticipated by Lee, U.S. Patent No. 5,487,037 ("Lee"). Applicants thank the Examiner for an explicit and clear description of how Lee is being read. However, Applicants respectfully traverse this rejection with respect to all claims.

Independent Claim 1

Applicants have amended Claim 1 to recite a programmable interconnection interposed between a first current-carrying terminal of a memory transistor and first and second bit nodes; and that the programmable interconnection connects the first current-carrying terminal of the memory transistor to the first bit node when programmed in a first state, and connects the first current-carrying terminal of the memory transistor to the second bit node when programmed in a second state. Applicants respectfully submit that Lee does not teach or even suggest such features.

In particular, Fig. 11 of Lee merely shows a memory cell having two fuses 1130, each fuse coupled between a transistor 1140 and a single bit node. Thus, Lee does not disclose a programmable interconnection between a first current-carrying terminal of a memory transistor and first and second bit nodes, as required by Claim 1. Furthermore, in Lee, each of the fuses 1130 is initially in an "unblown" state where

they are conducting and form an electrical connection between their terminals. Fuse 1130 may later be "blown," breaking the electrical connection and forcing the fuse in a non-conducting state. See Lee at col. 10, lines 11-15. Thus, it would be impossible for either of fuses 1130 of Lee to connect a terminal of a memory transistor to a first bit node when programmed in a first state, and connect the terminal to a second bit node when programmed in a second state, since Lee's fuse is non-conducting in one of its states and thus does not connect anything when in that state.

Therefore, Lee does not disclose or even suggest the invention recited in Claim 1, and Applicants respectfully request allowance of Claim 1.

Claims 2, 4, and 12-17 depend, either directly or indirectly, from Claim 1, and thus include all of the limitations of Claim 1. Applicants believe Claim 1 is allowable for the reasons set forth above. Therefore, for at least the same reasons, Applicants believe Claims 2, 4, and 12-17 are also allowable, and allowance of such claims is respectfully requested.

Independent Claim 8

Applicants have voluntarily amended independent Claim 8 to recite a memory transistor having a first current-carrying terminal connected to one of first and second bit nodes, a second current-carrying terminal connected to one of first and second power supply nodes, and a memory-transistor control terminal; and a programmable interconnection interposed between the second current-carrying terminal of the memory transistor and the first and second power supply nodes. The amendment merely clarifies the original language, and makes explicit what was inherent in the claim as presented in the previous response from Applicants. Applicants respectfully submit that Lee does not teach or even suggest the features of Claim 8.

The Examiner states that Lee teaches all claimed features in Fig. 11, including: "a programmable interconnection (1130) interposed between the second current-carrying terminal (the source terminal of 1140) of the memory transistor and at least one of first and second power supply nodes (ground)."Applicants respectfully disagree. As can be plainly seen in Fig. 11 of Lee, fuses 1130 are not interposed between the source terminals of transistors 1140 and ground. As shown in Lee, each of fuses 1130

is actually coupled between the drain terminals of 1140 and outputs of inverters 1110. As further clearly shown in Lee, the source terminals of transistors 1140 are directly connected to the ground node, without any interposing structure, much less a programmable interconnection. Thus, Lee fails to disclose or even suggest at least this feature of the claimed invention.

Therefore, since Lee fails to disclose at least one element of the invention recited in Claim 8, Applicants believe Claim 8 is allowable, and allowance of Claim 8 is respectfully requested.

Independent Claim 22

With respect to Claim 22, the Examiner stated that, in light of Lee, the array of configurable logic resources is "inherent; would be I/O logic circuits coupled to the input/outputs of the memory cells." Applicants respectfully disagree. Lee does not even mention, much less teach or disclose, configurable resources. In fact, nowhere in Lee are configurable resources, or any equivalent term, even mentioned. Furthermore, Claim 22 recites an "array of configurable resources," and Lee clearly does not disclose any such array. The Office Action fails to point out the supposed "I/O logic circuits" coupled to memory cells in Lee, and even assuming such circuits existed in Lee, there is clearly no array of such circuits. Applicants submit that there is no suggestion in Lee that any array of configurable logic resources is inherent, as alleged by the Examiner.

Moreover, in the interest of advancing prosecution, Applicants have voluntarily amended independent Claim 22 to recite that each memory cell further includes a configuration bit terminal, each configuration bit terminal coupled to at least one configurable logic resource in an array of configurable logic resources. Applicants respectfully submit that Lee does not teach or even suggest such features, and in fact teaches away from the invention. In particular, Lee does not disclose any memory cells having any terminal coupled to any circuit, much less memory cells having configuration bit terminals coupled to configurable logic resources. That is, even setting aside Lee's failure to disclose configurable logic resources noted above, there

is no teaching or suggestion in Lee that each memory cell has a terminal coupled to any circuit at all.

In fact, Lee merely describes a typical memory arrangement, well-known to those of ordinary skill in the art, having an array of memory cells and having decoding logic and a sense amplifier circuit, element 1034 in Lee, to read the memory cell. That is, Lee describes a memory 640 having 8 address lines to provide 16 select lines to select a column. Each column includes precharge transistors and pass gates to connect the column to sense amplifier 1034 when reading the memory. See, e.g., Lee at col. 8, lines 54-67. In contrast, Claim 22 recites a plurality of memory cells, each cell having a configuration bit terminal that is coupled to at least one configurable logic resource. Lee, in fact, teaches away from such an implementation by describing traditional column decoder and sense amplifier structures. Nowhere in Lee is it taught or suggested a memory cell has any bit terminal coupled to a configurable logic resource.

Therefore, Applicants believe Claim 22 is allowable, and allowance of Claim 22 is respectfully requested.

Claim 24 depends from Claim 22, and thus includes all of the limitations of Claim 22. Applicants believe Claim 22 is allowable for the reasons set forth above. Therefore, for at least the same reasons, Applicants believe Claim 24 is also allowable, and allowance of Claim 24 is respectfully requested.

Independent Claim 26

With respect to Claim 26, the Examiner stated that, in light of Lee, the configurable logic resources are "inherent; would be I/O logic circuits coupled to the input/outputs of the memory cells." Applicants respectfully disagree. As set forth above with respect to Claim 22, Lee does not teach or even suggest any configurable logic resources, and thus fails to anticipate Claim 26.

Furthermore, the Examiner alleged that Lee teaches all claimed features in Fig. 11, stating: "each memory cell including: a configuration bit node (one of cross coupled bit nodes) connected to one of the plurality of configuration bit terminals of the configurable logic resources and providing a configuration-bit signal (supplied by the

would be I/O logic circuits coupling to the input/outputs of the memory cells; inherent)." Applicants further respectfully disagree. As noted above with respect to Claim 22, Lee does not teach or even suggest any connection between memory cells and configurable logic resources, or any other circuit. That is, Lee merely describes a memory array arranged in columns having column select circuitry and sense amplifiers. See, e.g., Lee at col. 8, lines 54-67. Thus, the memory cells are coupled through bitlines through access transistors 1120, and there is no other connection to the memory cells of Lee.

Therefore, since Lee fails to disclose every element recited in Claim 26, Applicants believe Claim 26 is allowable, and respectfully request allowance of Claim 26.

Claim 28 depends from Claim 26, and thus includes all of the limitations of Claim 26. Applicants believe Claim 26 is allowable for the reasons set forth above. Therefore, for at least the same reasons, Applicants believe Claim 28 is also allowable, and allowance of Claim 28 is respectfully requested.

All of the above amendments are fully supported by the specification, for example in Figure 3 and the corresponding text.

Rejections Under 35 U.S.C. § 103

Claim 3 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee in view of Zhang et al., U.S. Patent No. 5,986,923 ("Zhang"). Applicants respectfully disagree and submit that Lee and Zhang, alone or in any combination, do not teach or suggest the claimed invention. Furthermore, Claim 3 depends from Claim 1, which is believed to be allowable for the reasons set forth above. Therefore, for at least the same reasons, Applicants believe Claim 3 is also allowable, and allowance of Claim 3 is respectfully requested.

Claims 6, 9, 25 and 27 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee in view of Raza, U.S. Patent No. 5,943,488 ("Raza"). Applicants respectfully disagree and submit that Lee and Raza, alone or in any combination, do not teach or suggest the claimed inventions. Furthermore, Claims 6

and 9 depend from Claim 1, Claim 25 depends from Claim 22, and Claim 27 depends from Claim 26. Each of Claims 1, 22, and 26 is believed to be allowable for the reasons set forth in greater detail above. Therefore, for at least the same respective reasons, Applicants believe Claims 6, 9, 25, and 27 are also allowable, and allowance of such claims is respectfully requested.

Objections

Claims 7, 10, and 11 are objected to as being dependent from a rejected base claim, but indicated as otherwise allowable. Applicants thank the Examiner for this acknowledgement of allowable subject matter. Claim 7 depends from Claim 1, and Claims 10 and 11 depend from Claim 8. Applicants believe Claims 1 and 8 are allowable for the reasons set forth above and that all rejections have been overcome. Therefore, Applicants believe the objections have also been overcome, and respectfully request allowance of Claims 7, 10, and 11.

Conclusion

No new matter has been introduced by any of the above amendments. In light of the above amendments and remarks, Applicants believe that Claims 1-4, 6-17, 22, and 24-28 are in condition for allowance, and allowance of the application is therefore requested. If action other than allowance is contemplated by the Examiner, the Examiner is respectfully requested to telephone Applicants' attorney, Justin Liu, at 408-879-4641.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patents, P.O. BOX 1450, Alexandria, VA 22313-1450, on October 13, 2005.

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Signature